

Different Implementation of Network Level in Embedded Networking with QoS

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Introduction



- Performance of modern embedded systems depends on network architecture and structure
- Many existing embedded networks standards provide QoS features, which are implemented by means of virtual channels (VC)
- We chose 3 approaches to implementation technology of VCs
- SpaceFibre standard is our case study

Structures of network level





1st way

- Quantity of connection points to the switch matrix for every port is equal to virtual channels number in this port
- Timing characteristics in the network layer depend only on arbitration rules

2nd way

- Quantity of connection points for every port
 = 1
- Impact between data flows and corresponding disturbance of its timing characteristics is more essential than in the 1st way

3rd way

- It is similar to 2nd way
- Packet transmission can be interrupted after N byte transfer



Network models



- 4 virtual channels
- Network
 - All terminal nodes (TN 1- 4) generate packets
 - Destinations are TN 1-4
 - The terminal nodes send the generated packets to each virtual channel
 - The destination nodes for each virtual channel are chosen randomly
 - VC1 has the highest priority, VC4 – the lowest





Average transmission time (1)



- Packet Size = 250 byte
- VC4 packet is generated first, then VC3 packet, then VC2 packet, then VC1 and so on repeated in loop. Delta between packet generation– 100 ns
- The average packet transmission time for three ways is almost similar



Average transmission time (2)



- Packet Size = 750 byte
- VC4 packet is generated first, then VC3 packet, then VC2 packet, then VC1 and so on repeated in loop. Delta between packet generation– 100 ns
- Timing characteristics of the 2nd way are worse in comparison with the 1st and 3rd way
- Timing characteristics of 3rd way are almost similar to the 1st way



Average transmission time (3)



- Exponential distribution of packet generation time
- Packet Size = 750 byte
- Average lower priority packet transmission time increases with growth of interruptions frequency

Theoretical & simulation results comparison



- Theoretical minimum delay is equal to simulation results
- Theoretical maximum delay is more than simulation delay



Hardware costs

Using Cadence RTL Compiler and Encounter and UMC 120 nm technology library

- 1st way
 - quantity of connection points > 4, hardware cost grows essentially
 - ➤ quantity of ports 16, quantity of virtual channels ≥ 16 the logical synthesis is impossible
 - ➢ quantity of ports ≥ 8, quantity of virtual channels ≥ 8 the physical synthesis is problematic
- 2st and 3rd way
 - It can be implemented with greater amount of virtual channels because 1 connection point per port is used

Switch matrix area(mm2)





Conclusion



- Timing characteristics of the 2nd way are worse in comparison with the 1st and 3rd way, if packet length is larger than the 256 bytes
- Average packet transmission time and achievable link utilization in case of 3rd way are almost similar to the 1st way
- 2nd and 3rd way have hardware costs less than 1st way
- The 3rd way is optimal from point of view of hardware costs and average packet transmission time



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DCNSimulator



- DCNSimulator is based on Qt and SystemC
- It consists of the simulation engine and libraries of network components
- In this study we used the router and node models which provide Virtual Channel mechanism and Network Layers only
- The results of the simulation can significantly depend on the router model implementation features (local clock frequency, link capacity)

