Introduction to Theory of the Real Time micro Operating Systems for embedded control systems

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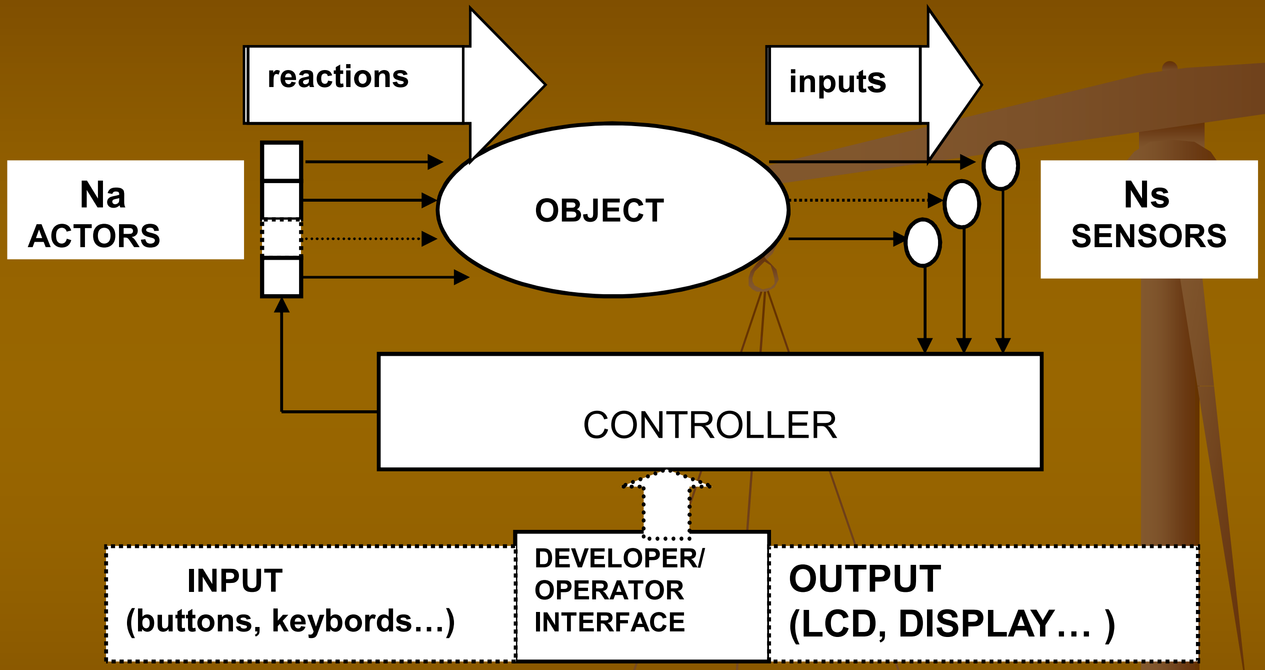
WHAT IS RTmOS ？

Simplified structure for the embedded multi channel control system



Classical theory defines the Real Time Control System as a system that provides reaction on object state changing or operator control commands during time that not exceed specified for every controlled channel

$$Tr_i < Tsp_i \quad i=1….Nch$$

WHAT IS RTmOS ?

Embedded control system has some specific features:

- **known number of control channels ;**
- **well determined algorithms for every channel;**
- **specified reaction time for every control channel;**

Embedded Control System for Hard Real Time Application

- **Control System for Hard Real Time Application supposes**
- **that every fault of control system can lead to un sufficient losses for end user;**
- **It means that for systems of this fault probabilities has to be specified;**

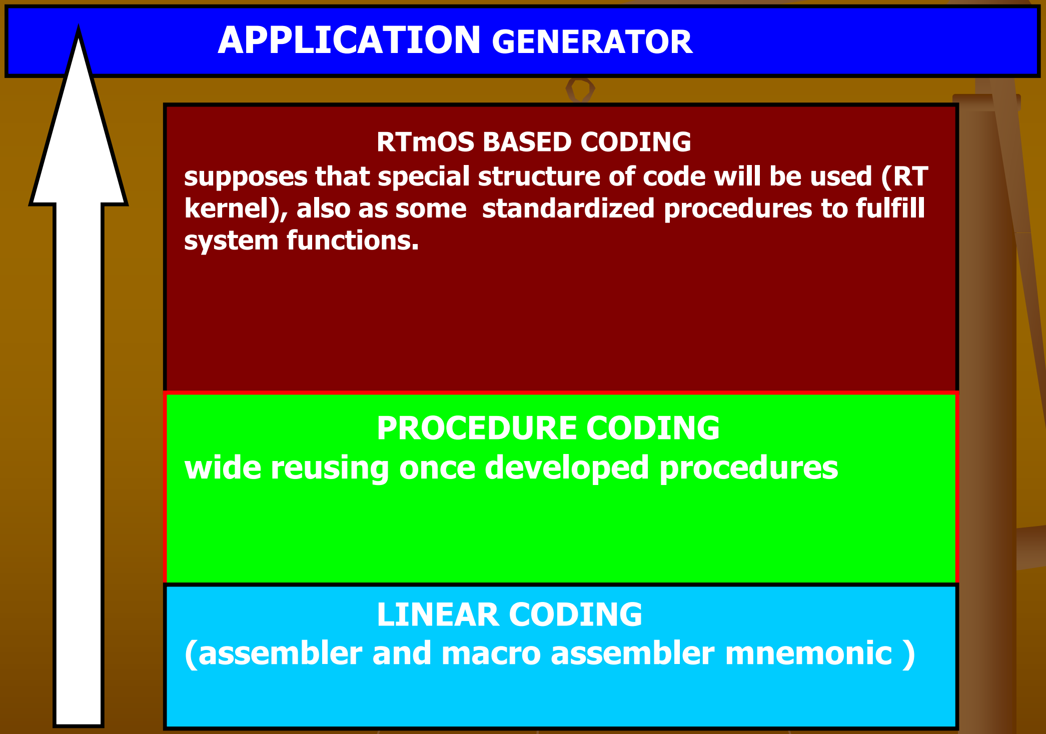
In Real Time Control Systems faults can occur due to:

- if some mistakes are exist in control algorithm for some channel;

- if specified reaction time is exceeded due to influence one channel on another;

WHAT IS RTmOS?

- **CODING IS PART OF DESIGNING AND HAS TO TREATED AS SOFISTICATED BUT TECHNOLOGY PROCESS;**
- **BASE OF THE MODERN CODING TECHNOLOGY;**



reliability

Increasing

APPLICATION GENERATOR

RTmOS BASED CODING

supposes that special structure of code will be used (RT kernel), also as some standardized procedures to fulfill system functions.

PROCEDURE CODING

wide reusing once developed procedures

LINEAR CODING

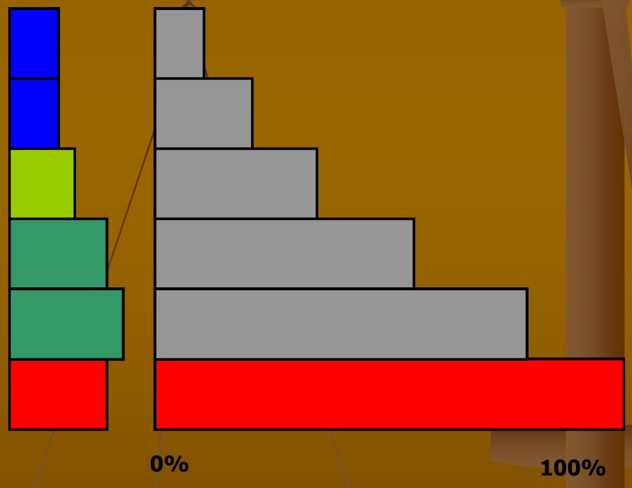
(assembler and macro assembler mnemonic)

- **RTmOS IS A KEY ELEMENT OF MODERN INTEGRATED DEVELOPMENT ENVIROMENTS (IDE);**

EMBEDDED SOFTWARE DESIGNING

- Software designing is a complex multiphase process;
- IDE is a basic tool and basic part of modern microcontroller platforms;

REQUIREMENT ANALYSES	**10%**
SYSTEM SPECIFICATION	**10%**
DESIGNING	**15%**
CODING	**20%**
AUTONOMOUS TESTING	**25%**
COMPLEX TESTING	**20 %**



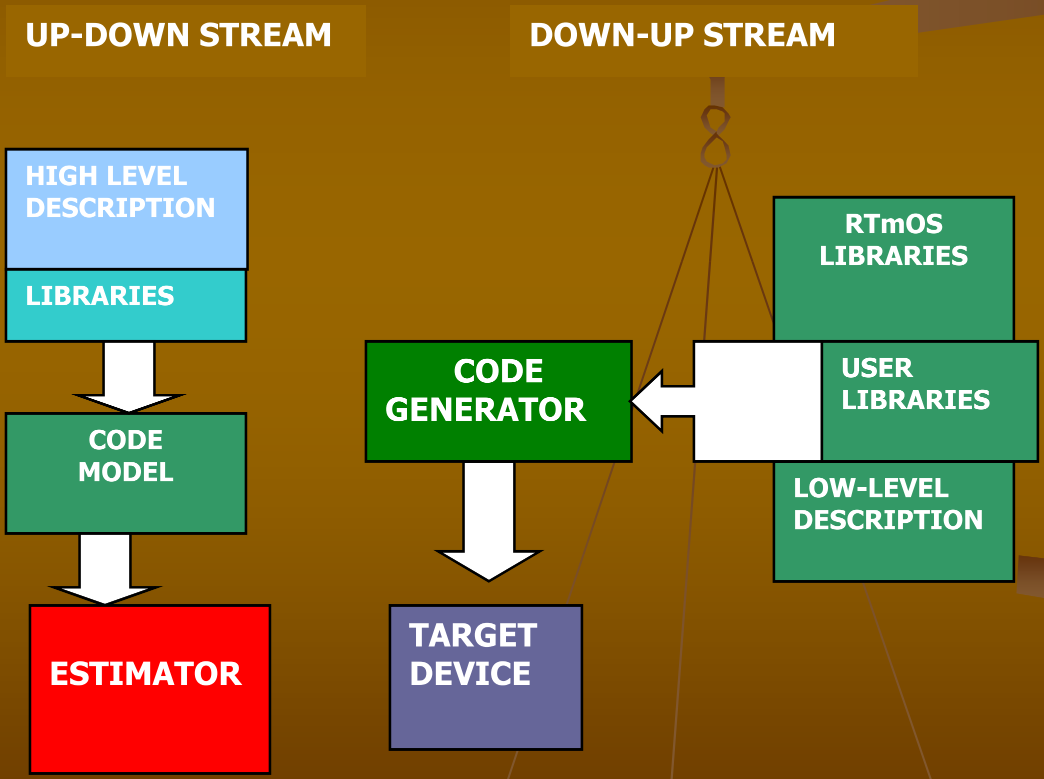
DESIGN PHASE

TIME EXPENCIES

- **TESTING TAKES AT LEAST 45% OF PROJECT`TIME (FOR GOOD DESIGN TEAM);**
- **TO REDUCE A PROJECT DURATION WE NEED A NEW TECHNOLOGY OF DESIGNING;**

WHAT EMBEDDD CONTROL TECHNOLOGY NEEDS ?

- To increase productivity and quality of systems the new generation of IDE has to be created;
- As the very first step the background theory for up-down stream has to be developed;



UP-DOWN STREAM

HIGH LEVEL DESCRIPTION

LIBRARIES

CODE MODEL

ESTIMATOR

DOWN-UP STREAM

RTmOS LIBRARIES

USER LIBRARIES

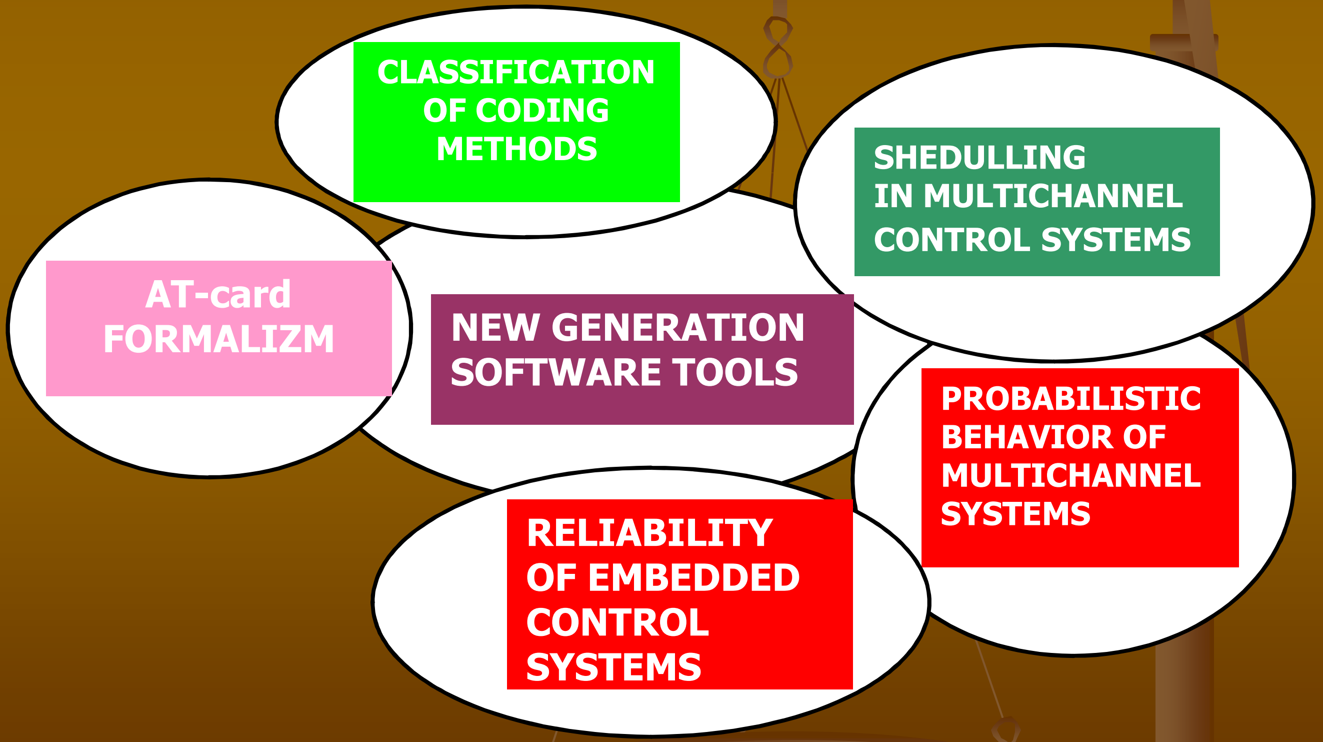
LOW-LEVEL DESCRIPTION

CODE GENERATOR

TARGET DEVICE

RTmOS THEORY STRUCTURE

- THEORY HAS TO ESTABLISH THE BASE FOR IDE OF THE NEXT GENERATION



CLASSIFICATION OF CODING METHODS

SHEDULLING IN MULTICHANNEL CONTROL SYSTEMS

AT-card FORMALIZM

NEW GENERATION SOFTWARE TOOLS

PROBABILISTIC BEHAVIOR OF MULTICHANNEL SYSTEMS

RELIABILITY OF EMBEDDED CONTROL SYSTEMS

AT –CARD FORMALIZM

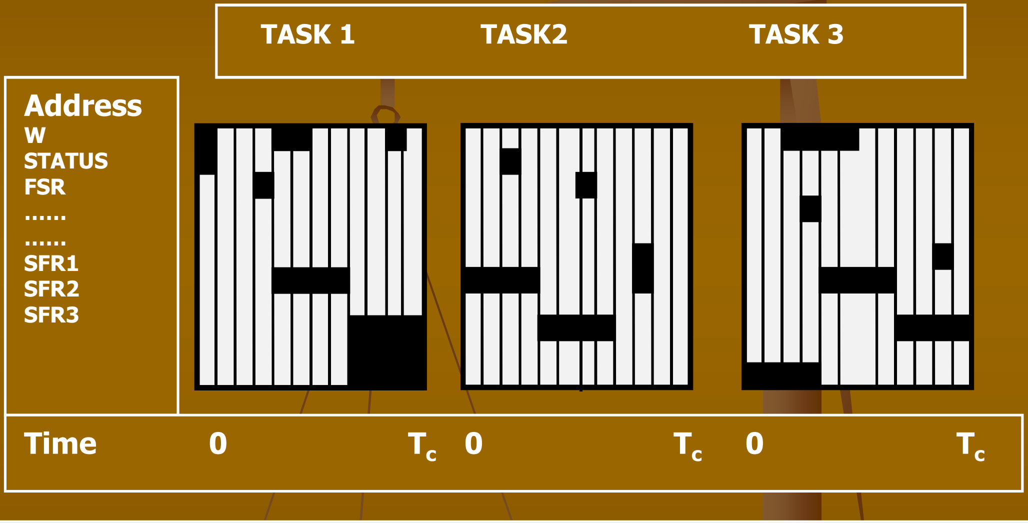
- **PHYLOSOPHY OF APPROACH:**

- **RT- CONTROL SYSTEMS FINAL CODE IS A MIXTURE OF RT-KERNEL SYSTEM AND USER FUNCTIONS THAT IS PRODUCED WITH SOME KIND OF APPLICATION GENERATOR ;**
- **FOR MULTI CHANNEL REAL TIME APPLICATIONS RESULTING CODE HAS TO FULFILLED SPECIFIED TIME REQUIREMENTS ALSO, AS FORMAL LOGIC REQUIREMENTS TO ALGORITHM FOR EVERY CONTROL CHANNEL;**
- **APPLICATION GENERATOR USES HIGH LEVEL DISCRIPTION FOR ALGORITHM OF WHOLE MULTICHANNEL CONTROL SYSTEM TO GENERATE MODEL THAT WILL BE USED TO ESTIMATE SPECIFIED SYSTEM PARAMETERS;**
- **NEW TYPE OF ALGORITHM DESCRIPTION HAS TO BE PROPOSED;**
- **AT-CARD FORMALIZM WAS INVENTED AS THE FIRST STEP IN THIS DIRECTION ;**

AT-MAP

- AT-map is a formal description of necessary resources (memory addresses and time slots) to perform task execution (i.e. processes' flow), represented as a rectangular matrix. For AT-model address axis is formed from all microcontroller resources (memory cells, pin-outs, OS objects, etc.), that are numbered in some way. Time axis is divided into intervals (seconds or command cycles) that are numbered also.

```
Start  call  TASK1
          call  TASK2
          call   TASK2
    goto Start
```



Examples of AT-maps. W, STATUS, FSR, SFRi registers has unique numbers.
Black rectangles correspond to 1, white ones correspond to 0

- Elements of AT-map can be bit (for binary AT-map) or integer (for byte AT-map) values.
- Binary AT-map is formed according to the next rule:

  if task uses I-th address during J-th time slot, element (I, J) of matrix is equal to 1,
  otherwise it equals to 0.
- AT-map with integer and real elements can be used for more sophisticated purposes.

CRITICAL SECTION ANALYSIS PROBLEM with AT-card description

- **Definition 1:** AT-conflict between processes exists, if the different processes have to use the same address during the same time slot.

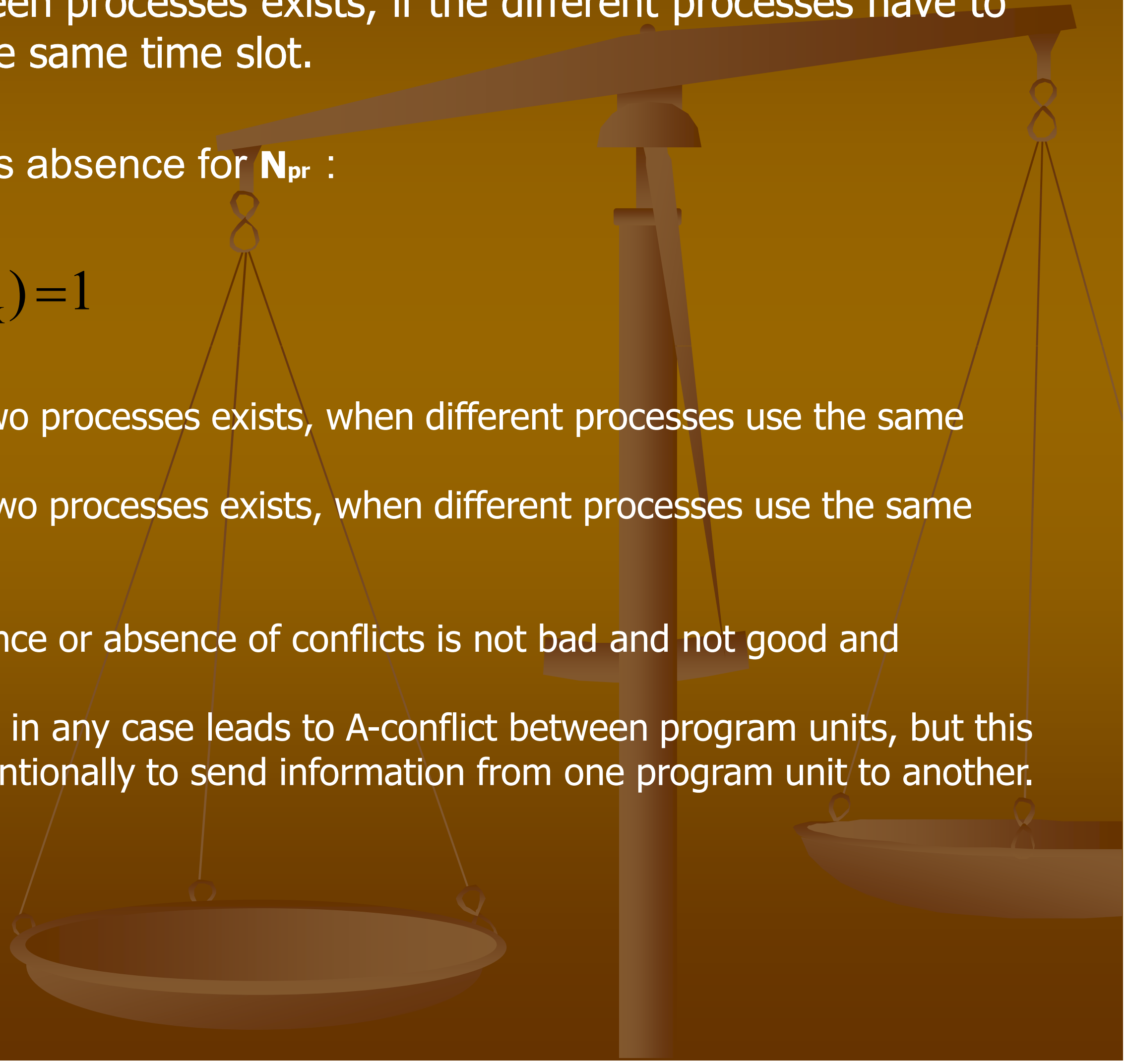
•Formal criterion of AT-conflict's absence for **N_{pr}** :

$$\max_{i,j}\sum_{k=1}^{N_{PR}}(AT_k)=1$$

- **Definition 2:** A-conflict between two processes exists, when different processes use the same address.
- **Definition 3:** T-conflict between two processes exists, when different processes use the same time slot.

- It has to be pointed out, that presence or absence of conflicts is not bad and not good and it depends on application.

  As example, global variable in any case leads to A-conflict between program units, but this conflict is   introduced intentionally to send information from one program unit to another.



BASIC IDEAS OF AT-FORMALIZM

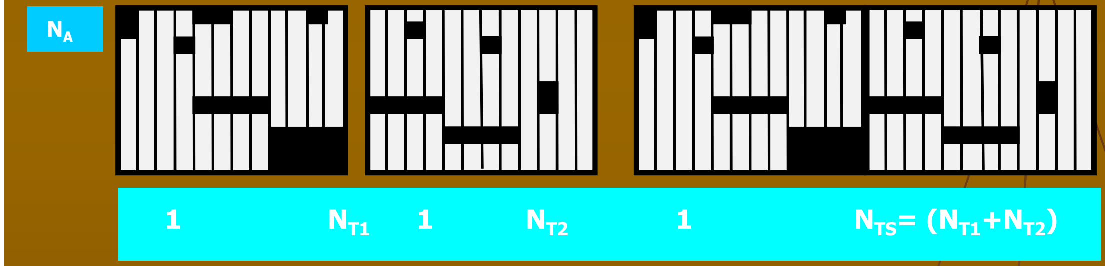
- Special formalizm (algebra ?) has to be developed for symbolic description

Description with classical matrix

Symbolical representation

AT_1 [union operation] AT_2 = ATc

Graphical representation



AT-map representation using sparse matrix technique

AT_1
[NA, NT1, N1] {i, j}

[union operation]

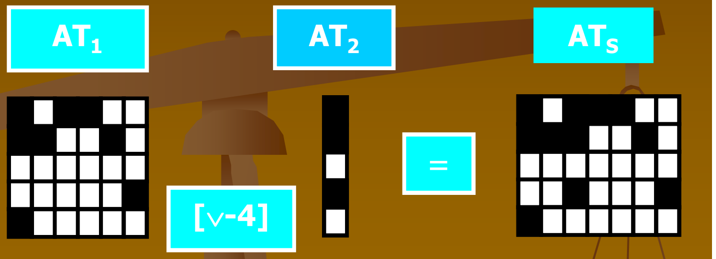
AT_2
[NA, NT2, N2] $\{i, j\}_2$

RESULT: AT_s [NA, NT1+NT2, N1+N2] $\{i, j\}_s$

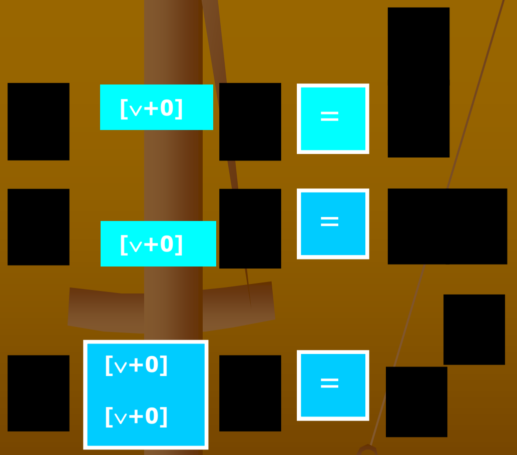
where $\{i,j\}_s$ = $\{i,j\}_1$, if k = 1 .. NT1

$\{i,j+ NT1\}_2$, if k = (NT1+1)…(NT1+NT2)

AT-formalism description



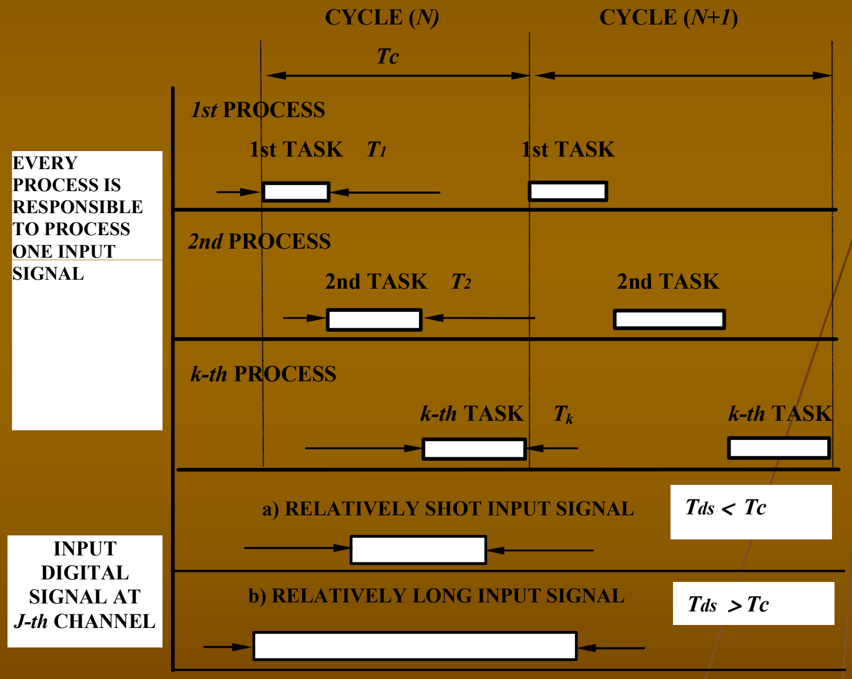
T- union operation using negative D parameter



T-union operation, A-union operation, AT-union operation

PROBABILISTIC BEHAVIOR OF MULTICHANNELSYSTEMS

- Reaction time has to be treated as probabilistic variable: step 1



EVERY PROCESS IS RESPONSIBLE TO PROCESS ONE INPUT SIGNAL

INPUT DIGITAL SIGNAL AT *J-th* CHANNEL

Fig. 4.1 FIFO dispatcher processogramma

Probability to miss input signal

$$T_r = T_c = \sum_{i=1}^{N_{ch}} T_i$$

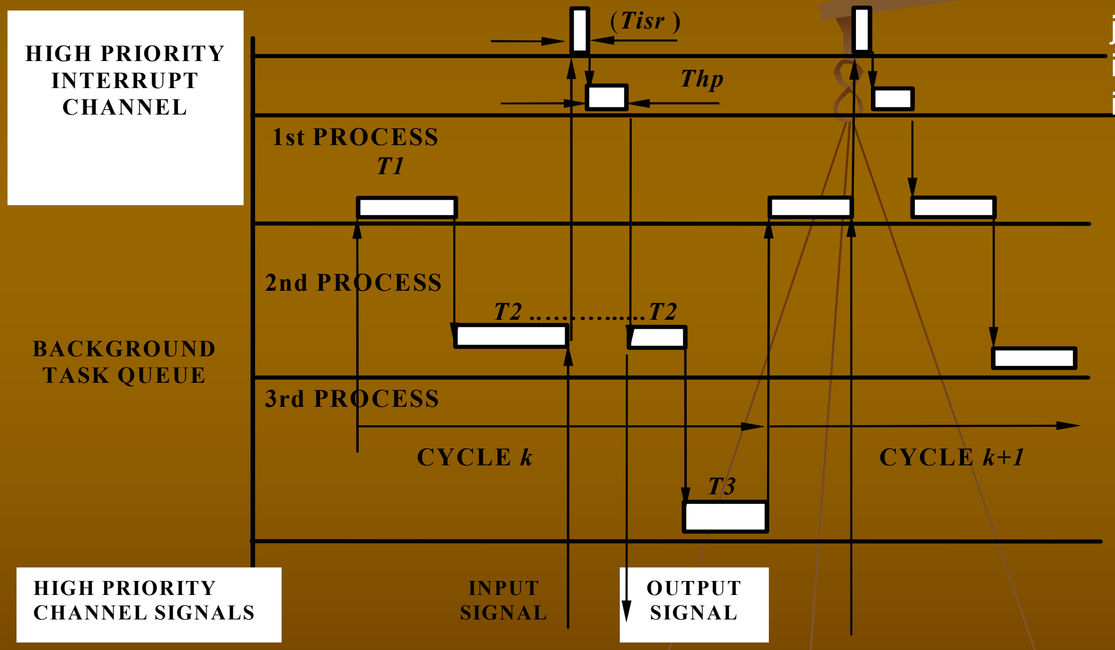
Probability to miss input signal

$$Pds_j = \frac{T_j + Tds}{T_c} \quad \text{for } \; 0 < \mathrm{Tds} < \mathrm{T_c} - T_j$$

$$Pds_j = 1 \quad \text{for } \; \mathrm{Tds} > \mathrm{T_c} - T_j$$

PROBABILISTIC BEHAVIOR OF MULTICHANNELSYSTEMS

- Reaction time has to be treated as probabilistic variable: step 2



Proccesogramma for interrupt-based system

OCS (**O**ne **C**hannel**S**ystem) The model supposes that the system has just one high-priority input channel that is describable as a Poisson flow with intensity

$\lambda =$ **1 / Tas,**

where **Tas** is the mean wait of input signal coming.

A stability condition for OCS can be formulated as

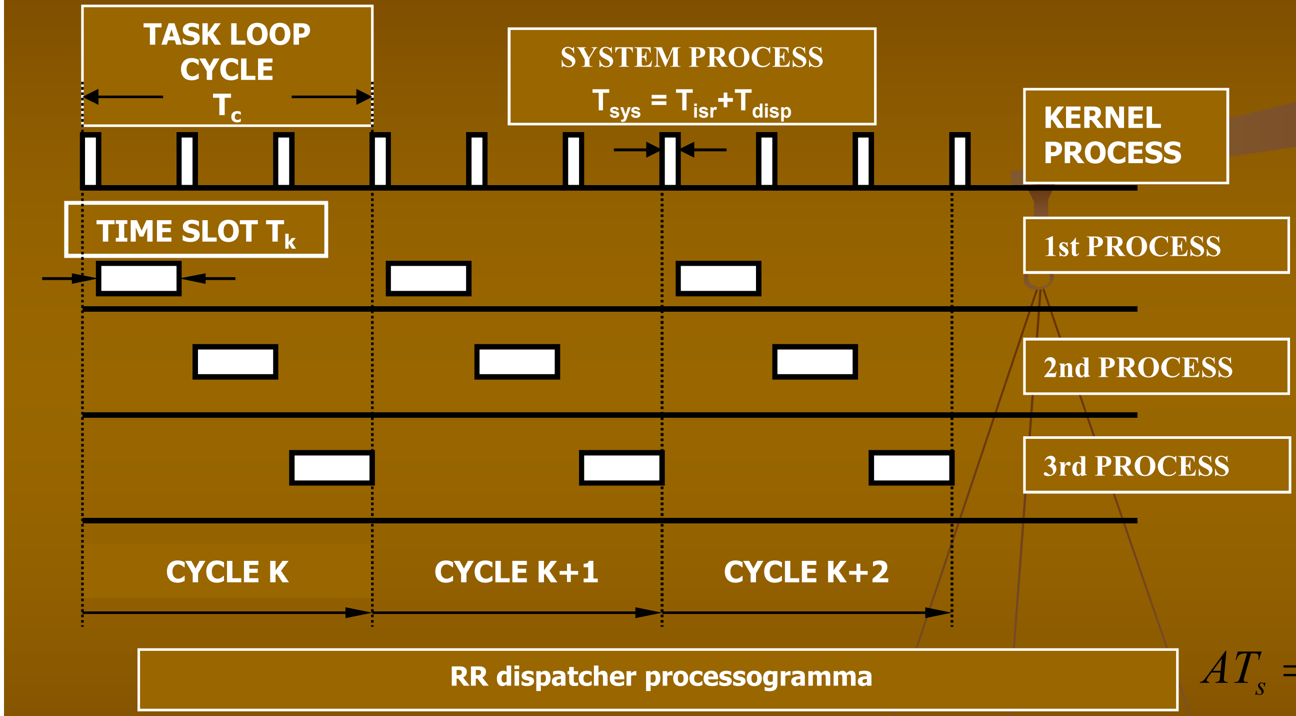
Tas = Ks Trhp, Ks >> 1

Probability of high-priority signal missing due to self blocking effect for **Ks >> 1** can be estimated as

$P_{fhp}(OCS) = 1 – (P(0,T_{rhp}) + P(1,T_{rhp}))$ and equal :

$$1-\left(\frac{1}{Ks}+1\right)e^{\frac{-1}{Ks}} \approx \frac{1}{Ks^{2}}$$

AT- MAP AND PROBABILISTIC BEHAVIOR OF MULTICHANNELSYSTEMS



Description with AT-formalism

$$AT_s = \sum_{k=1}^{\infty}{}_{[\vee+0]} (\sum_{i=1}^{N_{pr}}{}_{[\vee+0]} (AT_{sys}{}_{[\vee+0]} AT_i))$$

[⊥T] ATs

- **Probability analyses has to use projection operation**
- **Projection operations is a bridge to 1D interval algebras**
- **AT- map can be generalized for 3D and more dimensions**

PROBABILISTIC BEHAVIOR OF MULTICHANNELSYSTEMS

- **STATEMENT. The response time of multi-channel RTCS has to be interpreted as a probabilistic value:**

Trj = Trj (Pdsj)

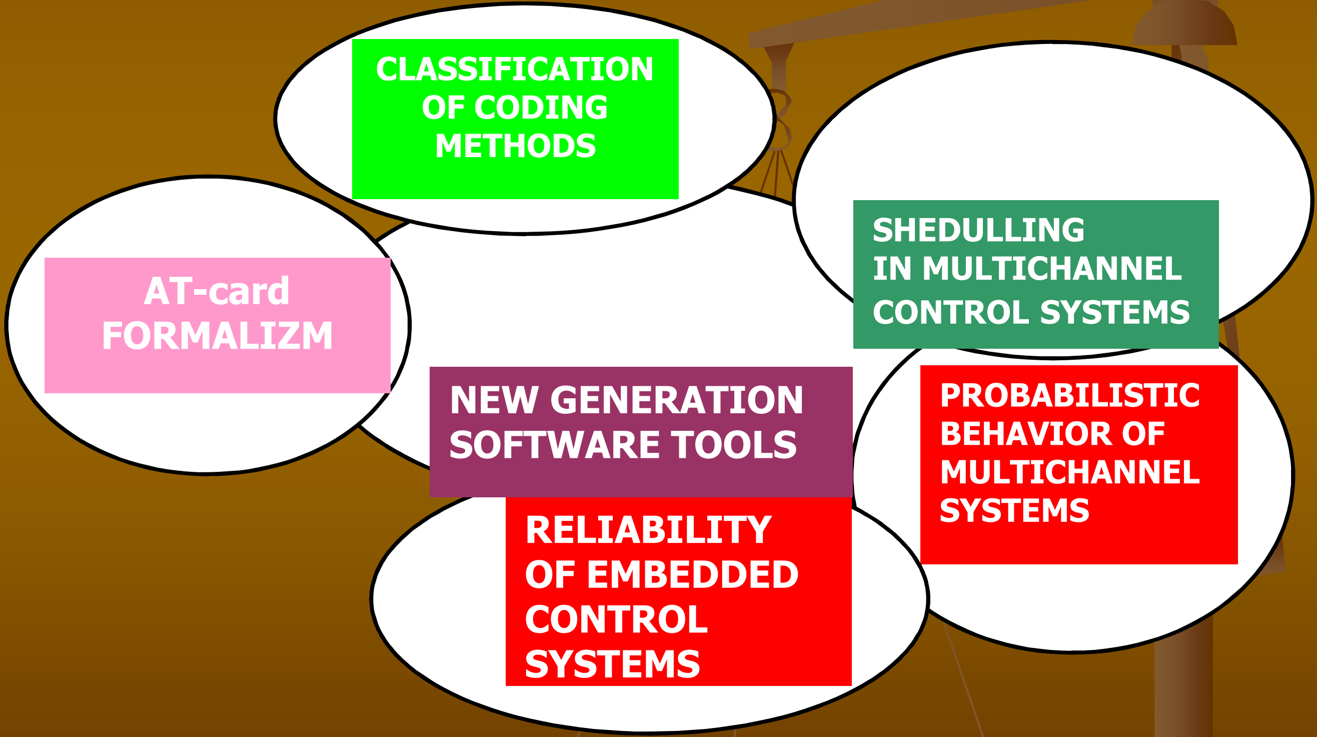
This statement changes the basic definition and means that the whole approach of software designing for real-time applications has to be changed thoroughly, at least for HRTA systems.

It has to be pointed out also that in real engineering practice it is necessary to take into account duration of initialization phase, abnormal conditions and so on.

  - **It means, that a question ”What is the probability of that the software developed for multi-channel RTSC will work properly?” has sense and great practical meaning.**

CONCLUSION

- THEORY HAS TO BE DEVELOPED FOR IDE OF THE NEXT GENERATION



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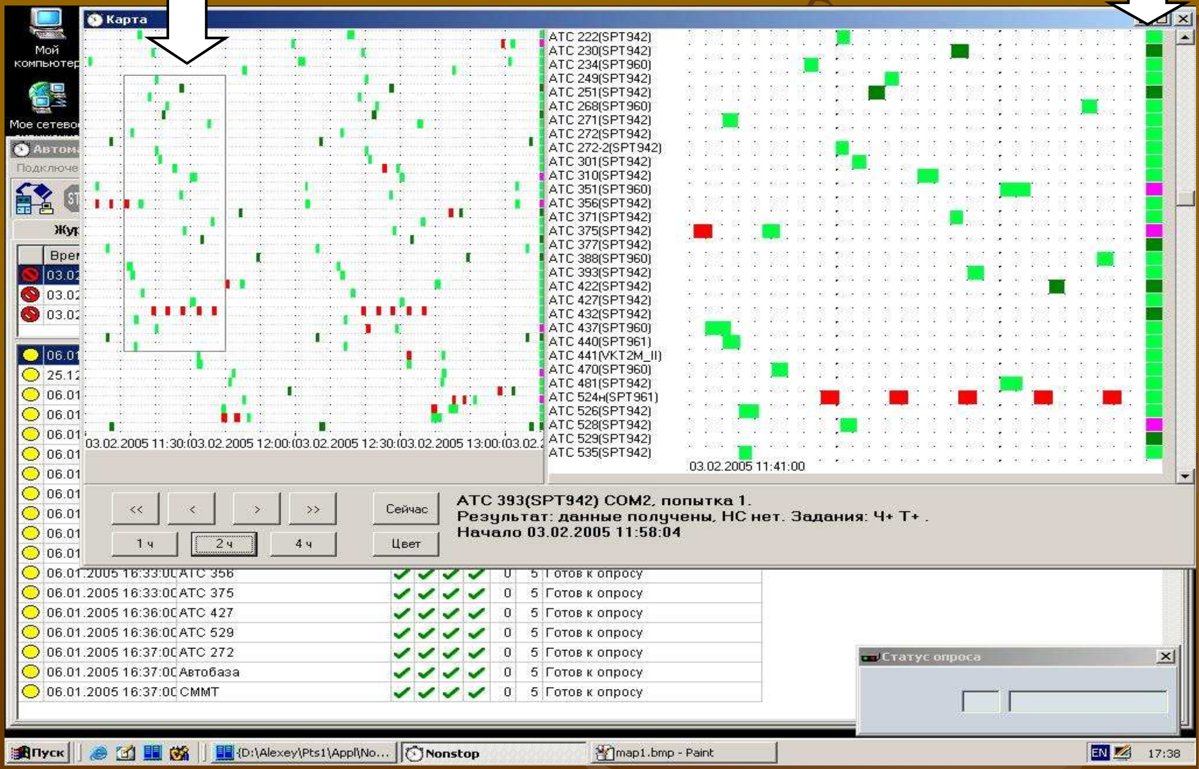
RELIABILITY OF EMBEDDED CONTROL SYSTEMS

- A LOT OF WORK HAS TO BE DONE, BUT THE VERY FIRST STEP HAS BEEN MADE

AT-MAP FOR USER INTERFACE DESCRIPIONS

Cutting operation
d3
[d1 □ d2] AT =   AT1
d4

Projection operation
[⊥ A] AT = AT2



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ATC 251(SPT942)
ATC 268(SPT960)
ATC 271(SPT942)
ATC 272(SPT942)
ATC 272-2(SPT942)
ATC 301(SPT942)
ATC 310(SPT942)
ATC 351(SPT960)
ATC 356(SPT942)
ATC 371(SPT942)
ATC 375(SPT942)
ATC 377(SPT942)
ATC 388(SPT960)
ATC 393(SPT942)
ATC 422(SPT942)
ATC 427(SPT942)
ATC 432(SPT942)
ATC 437(SPT960)
ATC 440(SPT961)
ATC 441(VKT2M_II)
ATC 470(SPT960)
ATC 481(SPT942)
ATC 524н(SPT961)
ATC 526(SPT942)
ATC 528(SPT942)
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ATC 535(SPT942)

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